IN THE CLAIMS:

Please amend claims 1-4 and add new claims 5-10 as follows:

1. (Currently Amended) A processor, comprising:

a memory for storing an instruction code and data;

an instruction code holding means for holding a plurality of instruction codes read from said memory;

a plurality of computing ~~units~~ devices operating in parallel according to the plurality of instruction codes held in said instruction code holding means;

~~an access port register file~~ a register file being shared by said plurality of computing devices, each of said plurality of computing devices reading/writing a content of said register file through a corresponding access port for computation;

a plurality of data memory banks each operated with at least one of said computing devices having means for issuing an instruction to load/store data to/from said access port register file, independently from other data memory banks; and

wherein one instruction code can be processed by the plurality of computing devices concurrently by designating, according to designation data in an instruction code stored in said memory, a plurality of the computing devices for executing said instruction code.

2. (Currently Amended) A processor comprising:

a memory for storing an instruction code and data;

an instruction code holding means for holding a plurality of instruction codes read from said memory; and

a plurality of computing ~~units~~ devices operating in parallel according to the plurality of instruction codes held in said instruction code holding means;

~~an access port register file~~ a register file being shared by said plurality of computing devices, each of said plurality of computing devices reading/writing a content of said register file through a corresponding access port for computation; and

a plurality of data memory banks each operated with at least one of said computing devices having means for issuing an instruction to load/store data to/from said access port register file, independently from other data memory banks;

wherein said computing devices ~~has~~ have at least an integer computing device, and a computing device operating operands including data other than integers; and

wherein one instruction code can be processed by the plurality of computing devices concurrently by designating, according to designation data in an instruction code stored in said memory, a plurality of the computing devices for executing said instruction code.

3. (Previously Presented) A processor according to claim 1, wherein at least one of said computing devices can execute a data transfer instruction for transferring data between said memory and said register file.

4. (Previously Presented) A processor according to claim 2, wherein at least one of said computing devices can execute a data transfer for transferring data between said memory and said register file.

5. (New) A processor according to claim 1, wherein:

one instruction code can be processed by the plurality of computing devices by designating a plurality of the computing devices for executing the instruction code through analysis of said designation data and inputting the instruction code into the designated plural computing devices.

6. (New) A processor according to claim 2, wherein:

one instruction code can be processed by the plurality of computing devices by designating a plurality of the computing devices for executing the instruction code through analysis of said designation data and inputting the instruction code into the designated plural computing devices.

7. (New) A processor according to claim 1, wherein:

said designation data contains data for designating a computing device for executing the instruction code and another computing device for executing the same instruction as the instruction code; and

at least two computing devices among said plurality of computing devices can process one instruction code according to said designation data.

8. (New) A processor according to claim 2, wherein:

said designation data contains data for designating a computing device for executing the instruction code and another computing device for executing the same instruction as the instruction code; and

at lease two computing devices among said plurality of computing devices can process one instruction code according to said designation data.

9. (New) A processor according to claim 1, further comprising:

a means for creating as many copies of the same instruction code as said instruction code as the designated plurality of computing devices according to said designation data, and inputting the created instruction codes into said instruction code holding means.

10. (New) A processor according to claim 2, further comprising a means for creating as many copies of the same instruction code as said instruction code as the designated plural computing devices according to said designation data, and inputting the created instruction codes into said instruction code holding means.